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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/667,906	09/22/2003	Joon-Hoo Choi	21C-0071	9911

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EXAMINER	
CHOW, DOON Y	
ART UNIT	PAPER NUMBER
2629	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/667,906	CHOI ET AL.	
	Examiner	Art Unit	
	Dennis-Doon Chow	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 June 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) *35-41* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14,17,18 and 23-34* is/are rejected.

7)☒ Claim(s) *15,16 and 19-22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 23-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 23 recites the limitation "the fifth thin film transistor" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Specification

3. The specification is objected to as failing to provide proper antecedent basis for the claimed subject matter.

Claim 26, lines 5-7 recites "a corresponding OLE diode in association with ... a pair of the data lines". This limitation is not support by the specification. As shown in Fig. 3, only a data line (Dp) is connected in a pixel drive unit of an OLE diode. A data line (Dp+1) is shown in the drawing but not connect to anything. It appears that data line (Dp+1) is belonged to a next pixel drive unit of an OLE diode. The specification only provides support for **a data line** in association with a corresponding OLE diode.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1-4, 6-11, 13-14,17-18 are rejected under 35 U.S.C. 102(b) as being anticipated (US 2002/0118150) by Kwon.

Regarding to claim 1, Kwon discloses an apparatus for providing a driving signal to an organic light emitting diode (Abstract) in an image display device, comprising: first and second control lines (select[n-1], select [n], Fig. 7) for transferring previous and current control signals, respectively, in a sequential process for providing the driving signal to the organic light emitting diode; a data line (Data[m], Fig. 7) for transferring a data signal for displaying images on the image display device; a first switching device (M3, Fig. 7) including a conduction path for transferring the data signal from the data line, the conduction path of the first switching device being controlled by the current control signal from the second control line (Select[n], Fig. 7); a second switching device (M4, Fig. 7) including a conduction path for transferring a reference signal externally supplied (ground, Fig. 7), the conduction path of the second switching device being controlled by the previous control signal from the first control line (select [n-1], Fig. 7, [0063]); a third switching device (M2, Fig. 7) including a conduction path for transferring the data signal provided from the first switching device, the conduction path of the third switching device being controlled by a state of the second

switching device; and a fourth switching device (M1, Fig. 7) including a conduction path for receiving a bias voltage (VDD, Fig. 7) and generating the driving signal to the organic light emitting diode, the conduction path of the fourth switching device being controlled by one of the reference signal from the second switching device and the data signal from the third switching device.

Regarding to claim 2, the third (M2, Fig. 7) and fourth (M1, Fig. 7) switching devices have switching characteristics substantially identical to each other.

Regarding to claim 3, Kwon further discloses a capacitor (C1, Fig. 7) for being charged with the bias voltage and for providing a voltage signal to control the conduction path of the third switching device.

Regarding to claim 4, wherein the first, second, third and fourth switching devices are first, second, third and fourth thin film transistors (see [0012] to [0016]), respectively, each having a conduction path between a source and a drain and a gate for receiving a control signal to control the conduction path; the first and second control signal lines are first and second gate lines, respectively; and the previous and current control signals are previous and current gate signals, respectively (see Fig. 7).

Regarding to claim 6, wherein the first thin film transistor has a gate to which the current gate signal is applied from the second gate line and a source and a drain to form the conduction path for transferring the data signal; the second thin film transistor has a gate to which the previous gate signal is applied from the first gate line and a source and a drain to form the conduction path for transferring the reference signal; the third thin film transistor has a gate to which the voltage signal from the capacitor is applied

and a source and a drain to form the conduction path for transferring the data signal; and the fourth thin film transistor has a gate to which one of the reference signal from the second thin film transistor and the data signal from the third thin film transistor is applied and a source and a drain to form the conduction path between the bias voltage and the organic light emitting diode (see Fig. 7).

Regarding to claim 7, wherein the conduction path of the second thin film transistor and the conduction path of the third thin film transistor are connected to the gate of the fourth thin film transistor and are parallel to each other with respect to the gate of the fourth thin film transistor (see Fig. 7).

Regarding to claim 8, wherein the gate of the third thin film transistor is connected with the gate of the fourth thin film transistor (see Fig. 7).

Regarding to claims 9-11, wherein the first and second thin film transistors are N-type thin film transistors, and the third and fourth thin film transistors are P-type thin film transistors (see Fig. 7), the third and fourth thin film transistors have a substantially identical negative threshold voltage.

Regarding to claim13, wherein an effective gate-source voltage of the fourth thin film transistor is dependent on the bias voltage and the data signal and independent of a threshold voltage of the fourth thin film transistor (see Fig. 7).

Regarding to claim14, wherein the bias voltage is provided from a power supply line disposed substantially parallel with the data line.

Regarding to claim17, wherein the source of the second thin film transistor is connected with the second gate line, so that the conduction path of the second thin film

transistor transfers the current gate signal to the fourth thin film transistor as the reference signal (see Fig. 7).

Regarding to claim18, wherein the bias voltage is provided from a power supply line disposed substantially parallel with the first and second gate lines (see Fig. 7).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 5, 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon.

Regarding to claim 5, Kwon does not explicitly disclose the thin film transistors are polysilicon thin film transistors. However, using a poysilicon material to make a thin film transistor is well known in the art. Thus it would have been obvious to one of ordinary skill in the art to use the known polysilicon thin film transistor as the thin film transistor in Kwon's apparatus since Kwon does not explicitly disclose using any specify thin film transistors.

Regarding to claim 12, Kwon does not explicitly disclose the reference voltage is equal to or larger than a gate-off voltage of the first thin film transistor and is equal to or

less than a sum of a threshold voltage of the third thin film transistor and a minimum voltage value of the data signal. However, as shown in Fig. 7, the reference voltage (ground) is equal to zero. The gate-off voltage of the first film transistor (M3, Fig. 7) is also equal to zero when the control line (select[n], Fig. 7) is not selected. The sum of a threshold voltage of the third thin film transistor (M2, Fig. 7) and a minimum voltage value of the data signal is obviously larger than Zero. Therefore, the reference voltage is equal to the gate-off voltage of the first thin film transistor (M3) and is less than the sum of the threshold voltage of the third thin film transistor (M2) and a minimum voltage value of the data signal.

8. Claims 26-27 and 30-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon.

Regarding to claim 26, Kwon discloses an organic light emitting display device comprising: a plurality gate lines (select[n] to select[n-2], Fig. 7) to which an active gate line is sequentially supplied; a plurality of data lines (D1-Dy, Fig. 4; Data[m], Fig. 7) to which data signals are applied to display images on the organic light emitting display device; and a plurality of pixel driving units each of which (Fig. 7) provides a driving signal to a corresponding OLE diode in association with a pair of the gate lines (select[n] and select[n-1]) and a data line (Data[m]), wherein each of the pixel driving units includes: a driving transistor (M1, Fig. 7) having a conduction path with one terminal receiving a bias voltage (VDD, Fig. 7) and the other terminal providing the driving signal to the diode; a first switching transistor (M4, Fig. 7) having a conduction

path for transferring a reference signal (ground, Fig. 7), the conduction path of the first switching transistor being controlled by a previous gate signal (see [0063]); and a second switching transistor (M2, Fig. 7) having a conduction path for transferring a data signal, the conduction path of the second switching transistor being controlled by a state of the first switching transistor, wherein the conduction path of the driving transistor is controlled by one of the reference signal from the first switching transistor and the data signal from second switching transistor.

Kwon does not explicit disclose the OLED diode associates with a pair of data lines. However, it is considered a matter of obvious design choice to have a pair of data lines in association with an OLE diode in Kwon's apparatus because this does not provide any unexpected result.

Regarding to claim 27, wherein a plurality of gate lines including a dummy gate line (select [n-2], Fig. 7) for providing a gate signal to the first switching transistor of a first one of the pixel driving units.

Regarding to claim 30, wherein each of the pixel driving units further includes a third switching transistor (M3, Fig. 7) having a conduction path for transferring the data signal from a corresponding one of the data lines to the second switching transistor, the conduction path of the third switching transistor being controlled by the current gate signal.

Regarding to claim 31, wherein the driving transistor and the second switching transistor have a substantially identical threshold voltage (see Fig. 7).

Regarding to claim 32, the display device further includes a plurality of power supply lines each of which is associated with a corresponding one of the pixel driving units for providing the bias voltage to the corresponding pixel driving unit, wherein the power supply lines are parallel with the data lines (see Fig. 7).

Regarding to claim 33, the display device further includes a plurality of power supply lines each of which is associated with a corresponding one of the pixel driving units for providing the bias voltage to the corresponding pixel driving unit, wherein the power supply lines are parallel with the gate lines (see Fig. 7).

Regarding to claim 34, wherein the driving, first and second switching transistors are thin film transistors each having a source and a drain forming a conduction path and a gate receiving a gate signal to control the conduction path (see Fig. 7).

9. Claims 28-29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kwon in view of Doliner et al. (4739320).

Kwon does not disclose simultaneously driving the dummy gate line and another gate line.

Doliner, in the same display field, discloses simultaneously driving two scanning lines.

In light of Doliner, it would have been obvious to one of ordinary skill in the art to simultaneously drive gate lines (scanning lines) so the speed of driving the display device can been improved.

Allowable Subject Matter

10. Claims15-16 and 19-22 objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

11. Claims 23-25 would be allowable if rewritten to overcome the rejection(s) under 35 U.S.C. 112, 2nd paragraph and the objection of the specification, set forth in this Office action and to include all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Dennis-Doon Chow whose telephone number is 571-272-7767. The examiner can normally be reached on 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Dennis-Doon Chow
Primary Examiner
Art Unit 2629

D. Chow
September 17, 2006